REMARKS

Reconsideration and favorable action therefor on the basis of the supported discussion and arguments submitted herewith is respectfully requested.

Although amendments are not being made to the previously pending claimed subject matter, an additional group of claims are being added thereto which similarly include the featured aspects of the stacked gate electrode of a MOS transistor contained with regard to the previously pending claims. The newly presented claims, however, are presented some what differently therefrom. For example, newly added independent Claim 33 calls for a semiconductor device which comprises, on a substrate, at least one MOS transistor, each of which having a gate electrode including the stacked structure similarly as that featured with regard to base Claim 1 as well as that of independent Claim 5. Moreover, newly added Claims 34 - 35 are similar to that of Claims 17 and 19 but, however, are combined with newly added Claim 33, respectively. Newly added dependent Claim 36 further limits the substrate of Claim 33 as including the semiconductor substrate. Newly added Claim 37 is similar to that of pending Claim 20 but, however, is combined instead with newly added independent Claim 33. Further, Claims 38 and 39 are also similar to Claims 17 and 19 but, however, are combined differently therefrom. Finally, newly added Claim 40 is similar to newly added Claim 36 but is combined differently therefrom. Discussions will now turn to the outstanding rejections.

Base Claim 1 as well as dependent Claims 3 - 4 and 17 - 21 thereof and, also, independent Claim 5 and dependent Claims 6 - 8 and 22 - 24 thereof were separately rejected under 35 U.S.C. § 103(a) over the teachings of Powell (US 6,265,297) "in view of the remark[s] "contained in the rejections. It will be shown, hereinbelow, the invention according to Claims 1+ and 5+ and, also, according to the

newly added Claims 33 - 40, was neither taught nor suggested by Powell nor, for that matter, even if one of ordinary skill were to have employed the rationale stated in the standing rejections. Therefore, insofar as presently applicable, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

In each of Claims 1+, 5+ as well as newly added Claims 33+, the gate electrode of a MOS transistor is configured as a stacked structure including a "silicon layer," a "metal silicide layer," a "reaction barrier layer," and a "metallic layer," formed in that order beginning with the silicon layer. With regard to the three example illustrations thereof of the present application (e.g., Figs. 1E, 2D, and 3D, although not limited thereto), the gate electrode stacked layers 103, 108, 105 and 106 are related thereto, respectively. Likewise, with regard to the fourth and fifth example embodiments of the present application, a similar such gate electrode stacked structure is provided (e.g., see in Figs. 5C and 7C the gate electrode stacked layer arrangement including n-polysilicon layer 311 and p-polysilicon layer 312 of the CMOS structure, metal silicide layer 320, metal nitride layer 308 and metallic layer 307). A detailed example regarding the particularities of each of the layers in the stacked gate electrode arrangement of the MOS transistor is given with regard to Claims 4 and 8 (see page 6, lines 4 - 19, of the Substitute Specification). It is submitted, such a scheme as that presently called for in Claims 1+, 5+ and 33+ not only was not disclosed by Powell but, moreover, could not have been suggested therefrom, even in the manner as that alleged in the standing rejections.

In the rejections regarding Claims 1+ and 5+, it is alleged that Powell disclosed a silicon layer (56), a metal silicide layer (54), a reaction barrier layer (52) and a metallic layer, formed in that order beginning with the silicon layer, as presently called for in

each of independent Claims 1 and 5 and, presumably, with regard to newly added independent Claim 33. However, the stacked series of layers including 56, 54, 52, and 50, in that order, beginning with the silicon layer 56, in Powell do not constitute a gate structure as that called for in independent Claims 1, 5 and 33 of the present invention, as will be shown hereinbelow.

With regard to the stacked gate electrode structure in Fig. 8 of Powell, layer 54 is a "metallic interlayer" which, according to Powell, is preferably a metal nitride layer such as a titanium nitride (TiN) layer and is not a "metal-containing layer," as is alleged in the rejections. (Column 4 lines 10 - 17 and 46 - 51, in Powell.) A metal nitride layer such as TiN layer is understood to mean a reaction barrier layer such as noted on page 7, lines 17- 18, of the Substitute Specification. Layer 52 is described as a metal layer of the stacked gate electrode structure in Powell (e.g., metal layer 52 may be a tungsten layer). However, the "metal interlayer 54" acts as barrier layer noting that it is typified by a metal nitride such as TiN, in Powell's stacked gate electrode structure.

In contradistinction with that taught by Powell, the present invention calls for a gate electrode stacked layer structure, such as for a MOS transistor, including a silicon layer/metal silicide layer/a reaction barrier/ a metallic layer in that order, beginning with the silicon layer (the silicon layer may be a polycrystalline layer) and with various other details thereof as called for by Claims 1+, 5+ and 33+. With regard to the first example illustration of the present invention, although not limited thereto, as shown in Fig. 1E of the drawings, stacked layers 103, 108, 105 and 106 are constituted by a polycrystalline silicon layer, a metal silicide layer (e.g., tungsten silicide layer), a metal nitride layer (which is a reaction barrier layer) and a metallic layer (e.g., W), respectively. The metal silicide layer, the barrier layer and the

uppermost metal may be constituted by other examples such as mentioned on page 10, lines 3-13, of the Substitute Specification, although not limited thereto.

In order to realize the structure of the present invention, using Powell's gate electrode structure as an example thereof, it would be necessary for Powell's stacked arrangement to include an additional layer, namely, a metal silicide layer, between the barrier layer 54 and the polysilicon layer 56. The numerical identifier 50 in Fig. 8 of Powell represents the overall gate stacked structure while layer 90 represents the cap layer thereof and not the upper metal layer of the gate structure as that of the present invention. In the rejections, it is alleged that layer 54 is a "metal-containing layer" which may be a metal silicide layer and that layer 52 represents a "reaction barrier layer" of the present invention. However, as shown hereinabove, using the details of Powell's disclosure as evidence thereof, layer 54, clearly, could not have been a metal silicide layer noting that it is a metal nitride layer which does not act as a metal layer but, rather, is a reaction barrier layer and that layer 52 is a metal layer (e.g., W) and not a barrier layer. Moreover, since the described "metallic interlayer 54" is, effectively, a reaction barrier layer in Powell's stacked gate electrode structure, thereby preventing a reaction between the upper titanium (Ti) metal layer 52 and the underlying silicon material of polysilicon layer 56, Applicants submit, it would be, practically, impossible to realize a reactive silicide layer therebetween.

A stacked four-layered gate electrode structure for a MOS transistor according to Claims 1+, 5+ and 33+, it is submitted, could not have been achievable from Powell's teachings. In other words, not only has Powell failed to teach a scheme as that presently called for in Claims 1+, 5+ and 33+, but, moreover, a prima facie case of obviousness, also, could not have been established from Powell's

disclosure in conjunction with that alleged in the standing rejections. For these and other reasons, the rejections are clearly improper and should be accordingly withdrawn.

The withdrawal of previously newly added Claims 25 - 32, for the reasons given on page two of the outstanding Office Action, is clearly noted. However, upon a careful inspection of those claims as well as a comparison thereof with the examined claimed groups including Claims 1+, Claims 5+ and, presumably, also newly added Claims 33+, Applicants, through their own representative contend that the earlier newly added Claims 25 - 32 should also have been examined. That is, Applicants disagree with the Examiner's contention that the invention according to Claims 25 - 32 and that of the examined claims are divisible under 35 U.S.C. § 121. That is, Applicants consider the invention according to the examined claim groups and, presumably, also with regard to the newly added Claims 33 - 40, and that of the withdrawn Claims 25 - 32 are related in terms of combination and sub-combination. According to USPTO policy, "[i]n order to establish that combination and sub-combination inventions are distinct, two-way distinctness must be demonstrated" and in order to "support a requirement for restriction, both two-way distinctness and reasons for insisting on restriction are necessary." MPEP § 806.05(c). Such clearly, it is submitted, has not been established in the outstanding Office Action.

In reading the details of the withdrawn Claims 25 - 32 and, in particular, base Claim 25 thereof, it is noted that the gate electrode structure thereof relating to both a MOS transistor of one channel conductivity type as well as a MOS transistor of a complementary channel conductivity type requires the specific details of the stacked gate electrode structure associate with a single MOS transistor such as that contained in Claims 1+, 5+ and 33+. Stated differently, the relationship between

independent Claim 25 (which is a combination claim including one MOS transistor and another complementary MOS transistor each having similar required details of the stacked gate electrode structure thereof) and, for example, independent Claim 1 (which is a specific sub-combination claim, i.e., a MOS transistor in which the gate electrode structure thereof is specifically detailed) is synonymous with the situation referred to in the manual as "AB_{sp}/B_{sp}," in which restriction is prohibited. That is, from a reading of the withdrawn Claims 25 - 32, the specific details thereof pertaining to either of the CMOS structure thereof are similar to that required in Claims 1+, etc. Applicants submit, therefore, such combination/sub-combination relationship as that noted above corresponds to a classical relationship (e.g., AB_{sp}/B_{sp}) in which a division between such claimed groups, under 35 U.S.C. § 121, would be improper.

Additionally, it is also urged that in view of the closeness of the subject matter between the examined claimed groups as well as that of the withdrawn Claims 25 - 32, as noted above, the Examiner is urged to also include Claims 25 - 32 for purposes of examination in connection with the mailing of a further official action on the merits (which is responsive to this submission). According the U.S. practice, further, and as set forth in MPEP § 803:

> "if the search and examination of an entire application can be made without serious burden, the Examiner must examine it on the merits, even though it includes claims to distinct or independent inventions."

It is submitted, therefore, that a close review of the claims, as has been discussed above, clearly shows that such close relationship does, in fact, exist between the different claims groups. Also, in view of the closeness of the claimed subject matter and the overlapping state-of-the-art searching that would obviously have to be performed, no serious burden would, it is submitted, be placed on the Examiner by

maintaining all of the above-discussed claims as a single group, at the present time, for purposes of examination. Moreover, Applicants would also be put under a serious burden in terms of both time and costs if they are required to file, unnecessarily, a still further application in order obtain complete coverage and patent protection on the various disclosed inventive aspects of the presently claimed subject matter. Accordingly, for these and other reasons, it is respectfully requested that withdrawn Claims 25 - 32 also be included in connection with the mailing of a further Office Action (which is responsive to the presently submitted amendment).

Therefore, in view of the amendments presented hereinabove together with the accompanying responsive remarks, reconsideration and favorable action on the previously rejected claims, along with the withdrawal of the standing restriction requirement directed to Claims 25 - 32 as well as a favorable action directed thereto, and an early formal notification of allowability of the above-identified application is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 500.40010X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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